REMARKS

This is intended as a full and complete response to the Office Action dated February 19, 2003, having a shortened statutory period for response set to expire on May 19, 2003. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-39 are pending in the application. Applicant confirms the election of claims 1-17. Claims 18-39 are withdrawn from consideration as being drawn to a non-elected invention. Applicants reserve the right to pursue the subject matter of claims 18-39 in a divisional application at a later date. Cancellation of claims 18-39 is not due to a concession that the claims are not patentable. Applicants present new claims 40-55 for consideration by the Examiner. It is believed that no new matter has been introduced in these claims.

Claim 2 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. The Examiner states that use of "the conductive material" in claim 2 fails to specify whether this is to be the first conductive material or second conductive material of claim 1. Applicants has amended claim 2 to recite "the first conductive material" and respectfully request allowance of claim 2. In addition, claims 4 and 15 have been amended to be properly dependent from a previous claim and includes aluminum as the second conductive material which is supported by the specification at least at paragraph 118, page 34, lines 26-30.

Claims 1-7 stand rejected under 35 U.S.C. § 102(e) as being anticipated by *Liu et al* (U.S. Pat No. 6,225,223). The Examiner states that *Liu et al.* '223 discloses a method for eliminating dishing of copper interconnects by forming a dielectric layer on a semiconductor substrate, forming trenches within the dielectric layer, depositing a barrier layer over the dielectric layer thereby lining the trench, depositing copper on the barrier layer to form a first copper layer filling the lined trench, planarizing the first copper layer and barrier layer thereby re-exposing the upper surface of the dielectric layer but also dishing the copper-filled trench, and selectively depositing copper on the dished copper-filled trench to form a second copper layer over the dished-copper-filled

trench and extending above the upper surface of the dielectric layer. Applicants respectfully traverse this rejection.

Liu et al. discloses a method of forming an interconnect including forming a barrier layer over a dielectric layer, depositing a first copper layer on the barrier layer to fill a trench, polishing both the first copper layer and barrier layer, exposing the surface of the dielectric layer and dished copper filled trench, and selectively depositing a second copper layer over the dished copper filled trench. Thus, the method of *Liu et al.* requires polishing both the first copper layer and barrier layer to expose the surface of the dielectric layer and dished copper filled trench in order to selectively deposit a second copper layer over the dished copper filled trench. Applicants respectfully point out that *Liu et al.* discloses polishing only the second copper layer in order to form a planar copper filled trench.

Liu et al. does not teach, show, or suggest polishing the first conductive material, to expose at least a top surface of the barrier layer material, as recited in claim 1 and claims dependent therefrom. Further, *Liu et al.* does not teach, show, or suggest depositing a second conductive material on at least the first conductive material to fill recesses formed in the first conductive material over the exposed top surface of the barrier layer material. Still further, *Liu et al.* does not teach, show, or suggest polishing both the second conductive material and the barrier layer material to expose at least a top surface of the dielectric layer to form a planar surface, as recited in claim 1 and claims dependent therefrom. Therefore, *Liu et al.* does not teach, show, or suggest subject matter as recited in claims 1-7. Withdrawal of the rejection is respectfully requested.

Claims 8-10 stand rejected under 35 U.S.C. § 103(a) as being obvious over *Liu et al.* as applied to claim 1 above, and further in view of *Iacoponi et al.* (U.S. Pat No. 6,489,240). The Examiner states that *Liu et al*, '223 teaches the above method for depositing and polishing various layers on a semiconductor substrate to form conductive interconnects but does not teach the use of annealing or rinsing steps nor the use of a manufacturing system having multiple processing stations. The Examiner also states that *Iacoponi et al.* teaches annealing of a deposited copper trench-fill layer to control the mechanical stress of the deposited copper layer (column 6, lines 23-46),

and *Iacoponi et al.* also teaches the use of a manufacturing system having multiple stations (column 9, line 58-column 10, line 4) with additional intermediate processing steps including rinsing (column 9, line 67).

As with the previous rejection, applicants respectfully traverse the rejection on grounds that the references cited by the Examiner, neither alone nor in combination, teach, show, or suggest the subject matter as recited in the claim 1 and claims dependent therefrom.

Liu et al. has been discussed above.

Iacoponi et al. discloses a method of forming a copper interconnect having multiple dielectric layers and multiple copper layers. The method of *Iacoponi et al.* includes forming a copper seed layer 525B and a copper layer 640, and annealing the copper layer 640 using a rapid thermal anneal process or a furnace anneal process (column 5 and column 6). In addition, *Iacoponi et al.* discloses the use of intermediate tools for performing various steps involved after the overall copper interconnect is formed, such as cleaning, rinsing, and forming additional layers (column 9, line 66-67). Further, *Iacoponi et al.* also discloses etching a roughened surface of a copper portion 740 by a selective etchant and depositing a thin copper layer 1100 above the copper portion 740.

However, *Iacoponi et al.* does not teach, show, or suggest polishing the first conductive material to at least a top surface of the barrier layer material, depositing a second conductive material by an electrochemical deposition technique on at least the first conductive material to fill recesses formed in the first conductive material, and polishing the second conductive material and the barrier layer material to at least a top surface of the dielectric layer to form a planar surface, as recited in claims 1 and claims dependent therefrom. Thus, *Liu et al.* in view of *Iacoponi et al.* does not teach, show, or suggest all of the limitations of claims 8-10, which are dependent from claim 1. Applicants respectfully request withdrawal of the rejection of claims 8-10.

Claims 11-17 stand rejected under 35 U.S.C. § 103(a) as being obvious over *Liu et al.*, in view of *Iacoponi et al.*, and further in view of *Zhang* (U.S. Pat. No. 6,341,998). The Examiner states that *Liu et al.* '223 teaches a method of depositing and polishing various layers on a semiconductor substrate to form conductive interconnects. *Iacoponi*

et al. teaches a method of forming conductive interconnects including steps for annealing and rinsing the workpiece, and also the use of a manufacturing system having multiple stations for performing the various process steps. However, neither reference teaches the concurrent deposition and polishing of a conductive layer. The Examiner also states that *Zhang* teaches a method for concurrent deposition and polishing of a conductive layer, which facilitates the efficient manufacture of electrical interconnections between components of an integrated circuit.

As with the previous rejection, applicants respectfully traverse the rejection on grounds that the references cited by the Examiner, neither alone nor in combination, teach, show, or suggest the subject matter as recited in the claims 1, 12, and claims dependent therefrom. *Liu et al.* and *Iacoponi et al.* have been discussed above. Both references do not teach, show, or suggest the method of the invention as recited in claims 1 and claims dependent therefrom. *Zhang* discloses an apparatus and a method for concurrent copper plating and polishing the plated copper on some portions of a wafer using a polishing pad to impede copper plating and facilitate plating/deposition in other desired locations of the wafer surface, such as an interconnect trench.

With regard to claim 11, *Liu et al.* and *Iacoponi et al.* do not teach, show, or suggest the method of the invention as recited in claims 1 and claims dependent therefrom. *Zhang* does not teach, show, or suggest elements lacking in *Liu et al.* and *Iacoponi et al.* with regard to claim 1 and claims dependent therefrom. Thus, *Liu et al.* in view of *Iacoponi et al.,* and further in view of *Zhang et al*, does not teach, show, or suggest all of the limitations of claim 11.

With regard to claim 12 and claims dependent therefrom, as pointed out by the Examiner, *Liu et al.* and *Iacoponi et al.* both fail to teach, show, or suggest an electrochemical deposition and polishing station disposed on the polishing system. In addition, *Liu et al.* discloses polishing only the second copper layer to form a planar copper filled trench and *Iacoponi et al.* discloses etching only the copper portion 740 and depositing a thin copper layer 1100 to form a planar copper filled trench. *Zhang* discloses concurrent copper plating and polishing the plated copper. Thus, all three references fail to teach, show, or suggest concurrent selective deposition and polishing of the conductive material and the barrier layer material. Specifically, the references fail

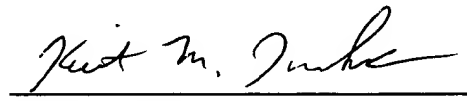
to teach, show, or suggest depositing a conductive material selectively on the copper containing material by an electroless deposition technique while removing the conductive material and the barrier layer material to at least a top surface of the dielectric layer by a polishing technique, as recited in claim 12 and claims dependent therefrom.

In addition, applicants respectfully point out that *Liu et al.* discloses polishing the first copper layer and the barrier layer and exposing the dielectric layer before depositing the second copper layer and *Iacoponi et al.* discloses annealing a copper layer, polishing the copper layer and a barrier layer, and exposing the dielectric layer before etching the copper layer. However, both references fail to teach, show, or suggest exposing the barrier layer to selectively deposit a conductive material on the copper material over at least a top surface of the barrier layer. *Zhang* does not teach, show, or suggest polishing a copper material from the substrate surface to at least a top surface of the barrier layer material, which is lacking in *Liu et al.* and *Iacoponi et al.* and as recited in claim 12 and dependent therefrom.

Thus, *Liu et al.* in view of *Iacoponi et al.,* and further in view of *Zhang et al*, does not teach, show, or suggest all of the limitations of claims 11-17. Applicants respectfully request withdrawal of the rejection of claims 11-17.

In conclusion, the references cited by the Examiner, neither alone nor in combination, teach, show, or suggest the method of the invention. The prior art made of record is noted. However, it is believed that the secondary references are no more pertinent to the Applicants' disclosure than the primary references cited in the office action. Therefore, it is believed that a detailed discussion of the secondary references is not deemed necessary for a full and complete response to this office action. Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,



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